

Abstract

Active protection circuit arrangement

5

A circuit arrangement for protecting integrated semiconductor circuits from electrical pulses or electrical overvoltages is proposed, said circuit arrangement having an RC element which comprises the 10 series circuit formed from a first resistor (R1; R10) and a capacitance (C1; C10) and is connected between two supply potential lines (VDD, VSS), having a chain of inverters (I10 - I12) which are connected in series behind one another, the input of said chain being 15 connected to the junction point between the first resistor (R1; R10) and the capacitance (C1; C10), and having a protection transistor (ST) whose control input is connected to the output of the inverter chain and whose outputs are connected to the two supply potential 20 lines (VDD, VSS).

Figure 2